

# SWITCHING N-CHANNEL POWER MOS FET

# DESCRIPTION

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The 2SK3634 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

### FEATURES

- High voltage: VDSS = 200 V
- Gate voltage rating: ±30 V R<sub>DS(on)</sub> = 0.60 Ω MAX. (V<sub>GS</sub> = 10 V, I<sub>D</sub> = 3.0 A)
- Low Ciss: Ciss = 270 pF TYP. (VDs = 10 V, VGs = 0 V)
- Built-in gate protection diode
- TO-251/TO-252 package
- Avalanche capability rated

### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (VGs = 0 V)	VDSS	200	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±30	V
Drain Current (DC) (Tc = $25^{\circ}$ C)	D(DC)	±6.0	А
Drain Current (Pulse) Note1	D(pulse)	±18	А
Total Power Dissipation (Tc = $25^{\circ}$ C)	Pt1	20	W
Total Power Dissipation ( $T_A = 25^{\circ}C$ )	Pt2	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	–55 to +150	°C
Single Avalanche Current Note2	las	6.0	Α
Single Avalanche Energy Note2	Eas	3.6	mJ
Repetitive Avalanche Current Note3	IAR	6.0	Α
Repetitive Pulse Avalanche Energy Note3	Ear	2.0	mJ

# CRDERING INFORMATION

PART NUMBER PACKAGE		
2SK3634	TO-251 (MP-3)	
2SK3634-Z	TO-252 (MP-3Z)	

(TO-251)



(TO-252)



#### **Notes 1.** PW $\leq$ 10 $\mu$ s, Duty Cycle $\leq$ 1%

- 2. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 100 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V, L = 100  $\mu$ H
- 3. Tch  $\leq$  125°C , Rg = 25  $\Omega,$  VDD = 100 V

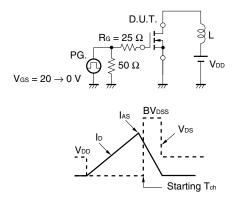
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# ELECTRICAL CHARACTERISTICS (TA = 25°C)

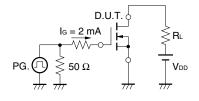
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	ldss	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	lgss	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	VGS(off)	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	2.5	3.5	4.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.0 A	2	4		S
Drain to Source On-state Resistance	RDS(on)	Vgs = 10 V, Id = 3.0 A		0.47	0.60	Ω
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		270		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V		75		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		33		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 3.0 A		4		ns
Rise Time	tr	V <sub>GS</sub> = 10 V		8		ns
Turn-off Delay Time	td(off)	R <sub>G</sub> = 0 Ω		14		ns
Fall Time	tr			6		ns
Total Gate Charge	QG	V <sub>DD</sub> = 160 V		9		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V		1.5		nC
Gate to Drain Charge	Qgd	I <sub>D</sub> = 6.0 A		4.5		nC
Body Diode Forward Voltage	VF(S-D)	IF = 16 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 6 A, VGS = 0 V		100		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		320		nC

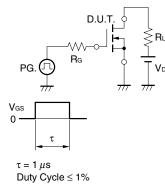
#### TEST CIRCUIT 1 AVALANCHE CAPABILITY

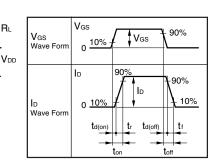
### **TEST CIRCUIT 2 SWITCHING TIME**

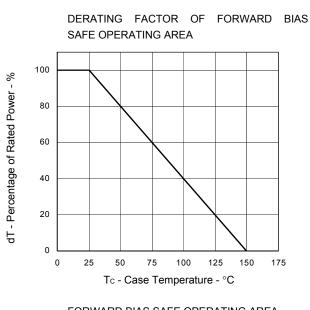


#### **TEST CIRCUIT 3 GATE CHARGE**



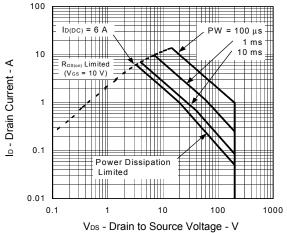


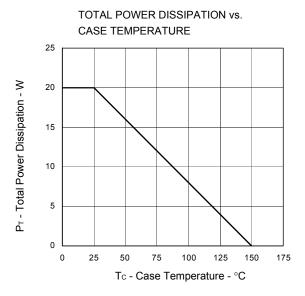




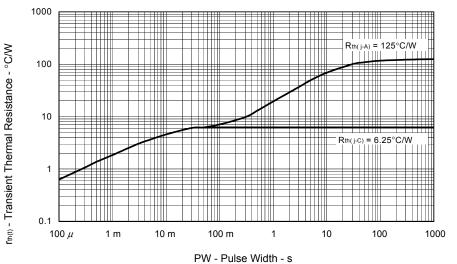
# TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)



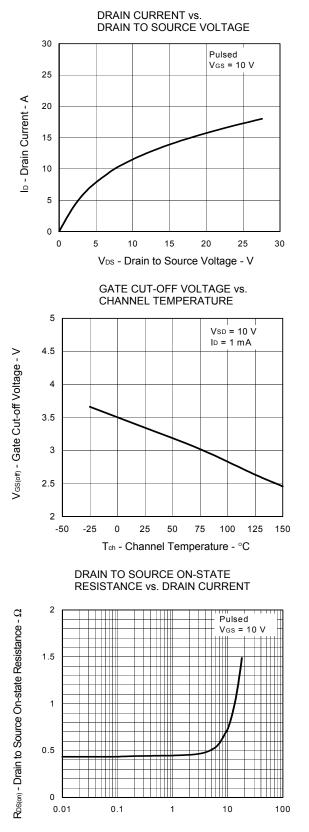




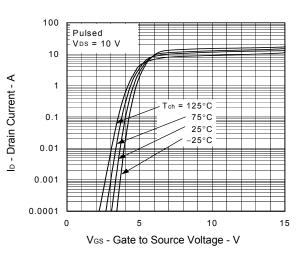




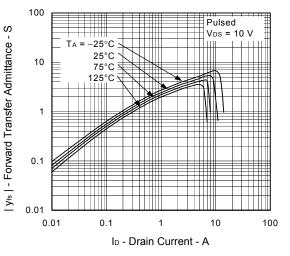




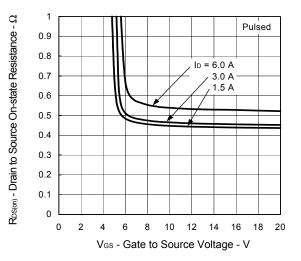
FORWARD TRANSFER CHARACTERISTICS



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



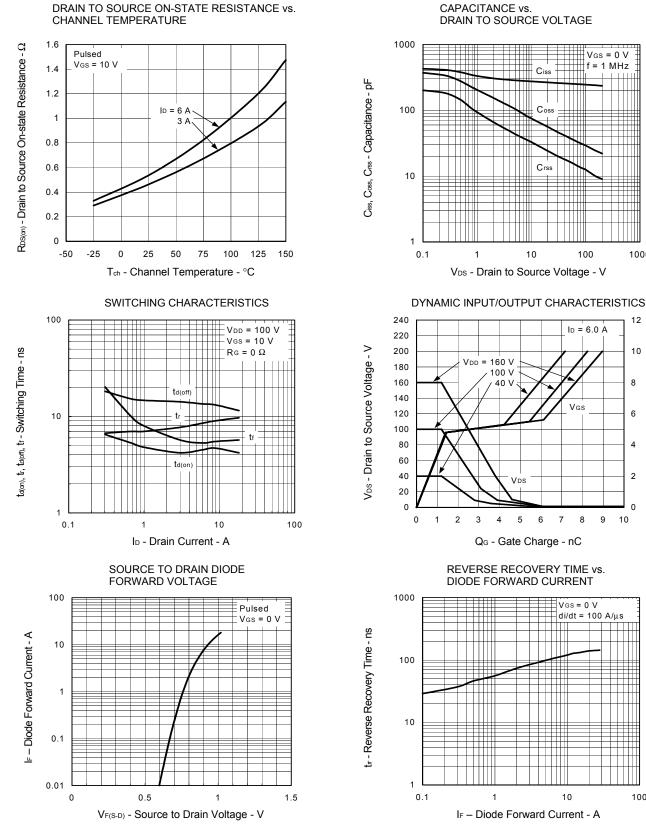
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



ID - Drain Current - A

Vgs = 0 V

f = 1 MHz



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#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

Ciss

Coss

Crss

10

100 V

40

ν

VDS

5

6 7

4

1

100

ID = 6.0 A

Vgs

8

VGS = 0 V

10

di/dt = 100 A/µs

9 10

1000

12

10

8

6

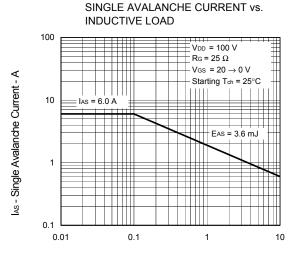
4

2

0

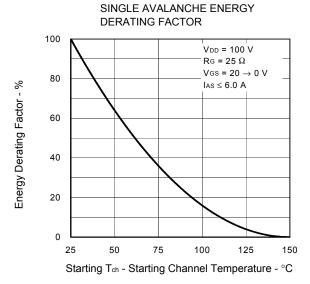


100

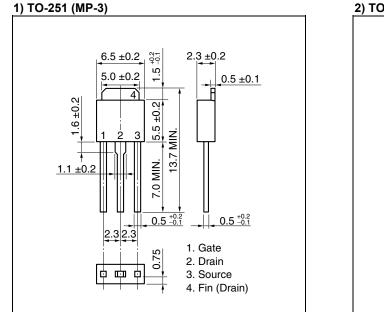


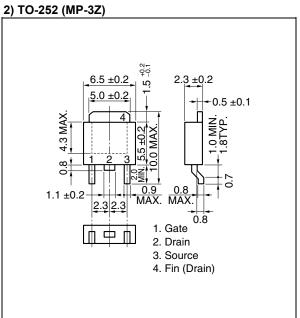
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L - Inductive Load - mH

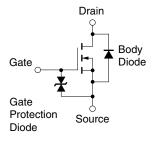


## ★ PACKAGE DRAWINGS (Unit: mm)





### **EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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